Docket No. 55561 (70820)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Y. Kubota et al.	CONF. NO.:	7275
U.S. SERIAL NO.:	09/775,167	EXAMINER:	S. Kumar
FILED:	February 1, 2001	GROUP:	2629
FOR:	SHIFT REGISTER CIRCUIT CAPABLE OF REDUCING CONSUMPTION OF POWER WITH REDUCED CAPACITIVE LOAD OF CLOCK SIGNAL LINE AND IMAGE DISPLAY DEVICE INCLUDING IT		

Mail Stop Appeal Brief—Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

BRIEF ON APPEAL

Sir:

This is an appeal from the final rejection of claims 1-25, as included in the Final Office Action mailed by the U.S. Patent and Trademark Office on September 21, 2007.

BRIEF ON APPEAL FEE

Authorization to charge Deposit Account No. 04-1105 for $510.00 is provided herewith to cover the appeal brief fee. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, the Commissioner is hereby authorized and requested to charge Deposit Account No. **04-1105**.

REAL PARTY IN INTEREST

The real party in interest is Sharp Kabushiki Kaisha. The assignment of the inventors to this corporation was recorded on February 1, 2001 at Reel 011516, Frame 0918.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to Appellant, Appellant's legal representative, or the assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 1-25 stand finally rejected. Claims 1-25 are appealed.

STATUS OF AMENDMENTS

No amendments have been filed after issuance of the Final Office Action.

A Pre-Appeal Brief Request for Review was filed on March 20, 2008. A Notice of Panel Decision from Pre-Appeal Brief Review issued on April 30, 2008, indicating that the application remains under appeal.

A clean set of the claims on appeal is set forth in the Claims Appendix hereto.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claims 1 and 25 are pending in the application.

Independent claim 1 recites "[a] shift register circuit provided with a plurality of register blocks each having a flip-flop that operates in synchronization with a clock signal and a transfer gate for controlling the clock signal supplied to the flip-flop, the plurality of register blocks being serially connected together." For example, as shown in FIG. 1 of the application, a plurality of flip-flops FF1 are "serially connected," and a transfer gate TG1 is provided for each flip-flop FF1 (see, e.g., specification at page 34, lines 3-7). A register block BLK1 includes the flip-flop FF1 and the transfer gate TG1 (see, e.g., page 34, lines 11-13). As stated on page 34, lines 10-11, "a clock signal CK is inputted to the flip-flops FF1 via this transfer gate TG1." As described in the specification, the shift register circuit of FIG. 1 "sequentially outputs output signals ... from the flip-flops FF1 in synchronization with the clock signal" (page 34, lines 18-22).

As further recited in independent claim 1, an input control signal of a transfer gate of a corresponding register block is "brought into an ON-state only in a specified period during which an output of the flip-flop of the corresponding register block changes." For example, with reference to FIGS. 1, 2C, and 2D of the application, an input control signal CTL1 of the transfer gate TG1 is brought into an ON-state only in a specified period during which the output OUT1 of the flip-flop FF1 changes (see, e.g., specification at page 35, lines 4-6). As shown in FIGS. 2C and 2D, the transfer gate is ON (see steps in FIG. 2C) only when an output OUT1 of the flip-flop changes (see slanted lines in FIG. 2D).

Independent claim 25 recites "[a] shift register circuit comprising a plurality of register blocks each having a flip-flop that operates in synchronization with a clock signal and a transfer gate for controlling the clock signal supplied to the flip-flop, the plurality of register blocks being serially connected together." For example, as shown in FIG. 1 of the application, a plurality of flip-flops FF1 are "serially connected," and a transfer gate TG1 is provided for each flip-flop FF1 (see, e.g., specification at page 34, lines 3-7). A register block BLK1 includes the flip-flop FF1 and the transfer gate TG1 (see, e.g., page 34, lines 11-13). As stated on page 34, lines 10-11, "a clock signal CK is inputted to the flip-flops FF1 via this transfer gate TG1." As described in the specification, the shift register circuit of FIG. 1 "sequentially outputs output signals ... from the flip-flops FF1 in synchronization with the clock signal" (page 34, lines 18-22).

As further recited in independent claim 25, a control circuit outputs a control signal to each of the transfer gates, the control signal being input to a transfer gate of a corresponding register block such that the control signal is "brought into an ON-state only when an output signal of the flip-flop of the corresponding register block changes." For example, with reference to FIGS. 1, 2C, and 2D of the application, an input control signal CTL1 of the transfer gate TG1 is brought into an ON-state only in a specified period during which the output OUT1 of the flip-flop FF1 changes (see, e.g., specification at page 35, lines 4-6). As shown in FIGS. 2C and 2D, the transfer gate is ON (see steps in FIG. 2C) only when an output OUT1 of the flip-flop changes (see slanted lines in FIG. 2D).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1-5, 14, and 25 are unpatentable under 35 USC §103(a) over U.S. Patent 5,289,518 to Nakao in view of "Applicant's Admitted Prior Art (AAPA)."

Whether claims 6, 9-12, 17-19, and 22-24 are unpatentable under 35 USC §103(a) over Nakao in view of "AAPA," and further in view of U.S. Patent 5,572,211 to Erhart et al. ("Erhart").

Whether claims 7 and 20 are unpatentable under 35 USC §103(a) over Nakao in view of "AAPA," further in view of Erhart, and further in view of U.S. Patent 5,602,561 to Kawaguchi et al. ("Kawaguchi").

Whether claims 8 and 21 are unpatentable under 35 USC §103(a) over Nakao in view of "AAPA," further in view of Erhart and Kawaguchi, and further in view of U.S. Patent 5,111,190 to Zenda.

ARGUMENT

The arguments contained herein pertain to the grounds of rejection listed above, i.e., independent claims 1 and 25 are not obvious over Nakao in view of "AAPA." In summary, independent claims 1 and 25 are patentable over the proposed combination of Nakao in view of "AAPA," and the final rejection should be vacated. Moreover, the remaining dependent claims are patentable over the cited references.

There is no teaching or suggestion in the proposed combination of Nakao in view of "AAPA" of a shift register circuit in which an input control signal of a transfer gate of a corresponding register block is brought into an ON-state only in a specified period when an output of the corresponding flip-flop changes, as recited in independent claims 1 and 25.

On pages 8-9 of the Final Office Action, the Examiner cited the following passage on page 7, lines 6-8 of the specification, which states: "only when the output of the flip-flop of each stage of the shift register circuit is significant (in an active state), a clock signal is inputted to the flip-flop."

Regarding the above passage of the Applicants' specification, the Examiner alleged: "thus when the output is not significant then it is not in the ON state, therefore teaching where the register block is brought into an ON state when the flip flop changes."

However, independent claims 1 and 25 require that an input control signal is brought into an ON-state **only** in a specified period during which an output of a flip-flop **changes**.

The above-cited passage of the specification (page 7, lines 6-8) refers to a prior art shift register circuit depicted in FIG. 39, where signal waveforms are shown in FIGS. 40A-40J and FIGS. 41A-41J. In particular, FIGS. 41A-41J were cited on page 3, lines 1-2 of the Final Office Action.

For example, referring to FIGS. 41C and 41D, the signal OUT1 represents an output signal, and the signal CTL1 represents a control signal (see specification at page 8, lines 3-9). It is apparent from FIGS. 41C and 41D of the application that the control signal CTL1 is not "brought into an ON-state **only** in a specified period during which an output [OUT1] of the flip-flop of the corresponding register block **changes**" (emphasis added), as recited in independent claim 1 (*see also* claim 25).

Instead, as shown in FIGS. 41C and 41D, the control signal CTL1 remains in an ON-state during the entire period in which the output OUT1 of the flip-flop is active, and thus is not

limited to the time period in which the output of the flip-flop changes, as required in independent claims 1 and 25.

There is simply no teaching or suggestion in the proposed combination of Nakao in view of "AAPA" of a shift register circuit in which an input control signal of a transfer gate of a corresponding register block is brought into an ON-state only in a specified period when an output of the corresponding flip-flop changes, as recited in independent claims 1 and 25.

Appellant submits that all of the claims under final rejection are in condition for allowance and should be allowed, and that the Final Office Action should be vacated.

Respectfully submitted,

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CLAIMS APPENDIX

Claim 1 (previously presented): A shift register circuit provided with a plurality of register blocks each having a flip-flop that operates in synchronization with a clock signal and a transfer gate for controlling the clock signal supplied to the flip-flop,

the plurality of register blocks being serially connected together, and

an input control signal of the transfer gate of a corresponding register block being brought into an ON-state only in a specified period during which an output of the flip-flop of the corresponding register block changes.

Claim 2 (original): A shift register circuit as claimed in claim 1, wherein

when a level of an input signal inputted to each register block and a level of an output signal outputted from the register block differ from each other, the transfer gate of the register block is brought into the ON-state.

Claim 3 (original): A shift register circuit as claimed in claim 1, wherein

the flip-flop is a D-type flip-flop, and

the register block has a logic operation section for executing a logic operation of an input signal of the register block and an output signal of the register block and controls the transfer gate to be turned on and off based on a signal representing a logic operation result of the logic operation section.

Claim 4 (original): A shift register circuit as claimed in claim 1, wherein

the flip-flop is an SR-type flip-flop,

the transfer gate is comprised of a first transfer gate for controlling input of the clock signal inputted to a set terminal of the SR-type flip-flop and a second transfer gate for controlling input of the clock signal inputted to a reset terminal of the SR-type flip-flop, and

the register block has a first logic operation section and a second logic operation section for executing a logic operation of an input signal of the register block and an output signal of the register block, controls the first transfer gate to be turned on and off based on a signal that represents a logic operation result of the first logic operation section and controls the second transfer gate to be turned on and off based on a signal that represents a logic operation result of the second logic operation section.

Claim 5 (original): A shift register circuit as claimed in claim 1, wherein

the register block has a retainment signal circuit that inputs to a clock input terminal of the flip-flop of the register block a retainment signal for bringing the output of the flip-flop into a retained state in a period during which the transfer gate is in an OFF-state.

Claim 6 (original): An image display device comprising a plurality of pixels arranged in a matrix form, a plurality of data signal lines for supplying image data to be written into the plurality of pixels, a plurality of scanning signal lines for controlling the image data to be written into the

pixels, a data signal line drive circuit for driving the data signal lines and a scanning signal line drive circuit for driving the scanning signal lines, wherein

at least one of the data signal line drive circuit and the scanning signal line drive circuit includes the shift register circuit claimed in claim 1.

Claim 7 (original): An image display device as claimed in claim 6, wherein

an output pulse width of the data signal line drive circuit is controlled by controlling a pulse width of an input signal inputted to the register block of the first stage of the shift register circuit.

Claim 8 (original): An image display device as claimed in claim 7, wherein

a side black region is displayed on an upper side and a lower side of an image display screen by writing a black signal into all the data signal lines while increasing the pulse width of the input signal inputted to the register block of the first stage of the shift register circuit so that all the data signal lines are brought into an active state by the data signal line drive circuit.

Claim 9 (original): An image display device as claimed in claim 6, wherein

at least one of the data signal line drive circuit and the scanning signal line drive circuit is formed on a substrate identical to that of the plurality of pixels.

Claim 10 (original): An image display device as claimed in claim 9, wherein

an active element constituting at least the data signal line drive circuit is provided by a polysilicon thin film transistor.

Claim 11 (original): An image display device as claimed in claim 10, wherein

the active element is formed on a glass substrate through a process at a temperature of not higher than 600°C.

Claim 12 (original): A shift register circuit as claimed in claim 1, wherein

the clock signal has a level lower than a clock signal input level of the flip-flop,

the register block has a level shift circuit for shifting a level of the clock signal so that the level of the clock signal becomes not lower than the clock signal input level of the flip-flop, and

the level shift circuit is brought into an operating state every register block only in a specified period during which the output of the flip-flop changes.

Claim 13 (original): A shift register circuit as claimed in claim 12, wherein

when a level of an input signal inputted to each register block and a level of an output signal outputted from the register block differ from each other, the transfer gate of the register block is brought into the ON-state, and

when a level of an input signal inputted to each register block and a level of an output signal outputted from the register block differ from each other, the level shift circuit of the

register block is brought into an operating state.

Claim 14 (original): A shift register circuit as claimed in claim 12, wherein

the register block has a retainment signal circuit that inputs to a clock input terminal of the flip-flop of the register block a retainment signal for bringing the output of the flip-flop into a retained state in a period during which the transfer gate is in an OFF-state.

Claim 15 (original): A shift register circuit as claimed in claim 14, wherein

the register block has an OFF-state signal circuit that inputs to the clock input terminal of the level shift circuit an OFF-state signal of a level at which no current flows through the level shift circuit in the period during which the transfer gate is in the OFF-state.

Claim 16 (original): A shift register circuit as claimed in claim 14, wherein

the level shift circuit is connected to a power source line and a ground line, and

the register block has a disconnecting circuit for disconnecting either one of the power source line and the ground line of the level shift circuit in the period during which the transfer gate is in the OFF-state.

Claim 17 (original): A shift register circuit as claimed in claim 12, wherein

the flip-flop is a D-type flip-flop, and

the register block has a logic operation section for executing a logic operation of an input

signal and an output signal of the register block and controls the transfer gate to be turned on and off based on a signal representing a logic operation result of the logic operation section.

Claim 18 (original): A shift register circuit as claimed in claim 12, wherein

the flip-flop is an SR-type flip-flop,

the transfer gate is comprised of a first transfer gate for controlling the input of the clock signal inputted to a set terminal of the SR-type flip-flop and a second transfer gate for controlling the input of the clock signal inputted to a reset terminal of the SR-type flip-flop, and

the register block has a first logic operation section and a second logic operation section for executing a logic operation of an input signal and an output signal of the register block, controls the first transfer gate to be turned on and off based on a signal that represents a logic operation result of the first logic operation section and controls the second transfer gate to be turned on and off based on a signal that represents a logic operation result of the second logic operation section.

Claim 19 (original): An image display device comprising a plurality of pixels arranged in a matrix form, a plurality of data signal lines for supplying image data to be written into the pixels, a plurality of scanning signal lines for controlling the image data to be written into the pixels, a data signal line drive circuit for driving the data signal lines and a scanning signal line drive circuit for driving the scanning signal lines,

at least one of the data signal line drive circuit and the scanning signal line drive circuit

includes the shift register circuit claimed in claim 12.

Claim 20 (original): An image display device as claimed in claim 19, wherein

an output pulse width of the data signal line drive circuit is controlled by controlling a pulse width of an input signal inputted to the register block of the first stage of the shift register circuit.

Claim 21 (original): An image display device as claimed in claim 19, wherein

a side black region is displayed on an upper side and a lower side of an image display screen by writing a black signal into all the data signal lines while increasing the pulse width of the input signal inputted to the register block of the first stage of the shift register circuit so that all the data signal lines are brought into an active state by the data signal line drive circuit.

Claim 22 (original): An image display device as claimed in claim 19, wherein

at least one of the data signal line drive circuit and the scanning signal line drive circuit is formed on a substrate identical to that of the pixels.

Claim 23 (original): An image display device as claimed in claim 22, wherein

an active element constituting at least the data signal line drive circuit is provided by a polysilicon thin film transistor.

Claim 24 (original): An image display device as claimed in claim 23, wherein

the active element is formed on a glass substrate through a process at a temperature of not higher than 600°C.

Claim 25 (previously presented): A shift register circuit comprising a plurality of register blocks each having a flip-flop that operates in synchronization with a clock signal and a transfer gate for controlling the clock signal supplied to the flip-flop,

the plurality of register blocks being serially connected together, and further comprising:

a control circuit outputting a control signal to each of the transfer gates, the control signal being input into the transfer gate of a corresponding register block such that the control signal is brought into an ON-state only when an output signal of the flip-flop of the corresponding register block changes.

EVIDENCE APPENDIX

Attachment A — Copy of U.S. Patent 5,289,518 to Nakao, as relied on by the Examiner in the Final Office Action.

Attachment B — Copy of U.S. Patent 5,572,211 to Erhart et al., as relied on by the Examiner in the Final Office Action.

Attachment C — Copy of U.S. Patent 5,602,561 to Kawaguchi et al., as relied on by the Examiner in the Final Office Action.

Attachment D — Copy of U.S. Patent 5,111,190 to Zenda, as relied on by the Examiner in the Final Office Action.

RELATED PROCEEDINGS APPENDIX

None.